



## onTAP'S USB TEST AND PROGRAMMING CABLE

*Offers Higher Speeds and Simplified Operation*

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### onTAP USB Test and Programming Cable



The onTAP USB Test and Programming Cable provides JTAG test and programming support for onTAP boundary-scan software. It is an ideal replacement for parallel port programming cables, offering higher speeds and simplified operation in both single and multiple chain applications with multiple chain applications requiring multiple USB cables.

The cable may be used for the following applications:

- JTAG Test, including memory and cluster test
- Flash programming
- FPGA, CPLD and PROM configuration
- General purpose PIO

The onTAP USB Cable offers either a ribbon cable header for direct connection to Xilinx, Altera and other style headers, or flying lead connectors which provide increased flexibility. The cable attaches to the USB port on a PC with a standard Hi-Speed USB A-A cable.

### Features

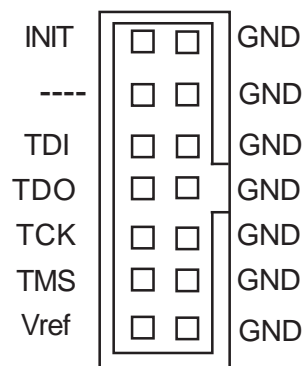
- Supported on onTAP and Windows
- Attaches to USB ports and hubs with off-the-shelf Hi-Speed USB A-A cables
- Derives all power from USB ports and hubs. Target board Vref voltage provides power only for JTAG pin drive
- Automatically senses and adapts to target I/O Voltages
- Interfaces to devices operating at 1.5 to 5.0 VDC
- JTAG pin currents +/- 24mA
- Adjustable TCK clock from 60KHz to 6MHz
- Drivers provided
- Compatible with Xilinx Platform Cable USB flying wire leads and High Performance Ribbon Cable
- JTAG pins compatible with the Xilinx Platform Cable USB, including TCK, TMS, TDI, and TDO. Tri-state, drive, and sense available on the INIT pin
- Cable adapter available for Altera and other custom headers
- Hot plug and play
- Operates in onTAP single chain and multi-chain / multi-cable JTAG applications
- LED indicators show status of both Vref and Cable voltages
- Suspend state or loss of Vref tri-states outputs on all pins
- Dimensions 3.54" x 1.97" x .94"

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## Ribbon Cable Connector



## Pinout Assignments

<i>Pin Name (JTAG)</i>	<i>Flying Lead Wire</i>	<i>Ribbon Cable</i>	<i>Description</i>
TDI	2	10	<b>Test Data In</b> This is the target serial input data stream for JTAG operations and is connected to the TDI Pin on the first device in the JTAG chain
TDO	3	8	<b>Test Data Out</b> This is the target serial output data stream for JTAG operations and is connected to the TDO pin on the last device in the JTAG chain.
TCK	5	8	<b>Test Clock</b> This is the clock signal for JTAG operations and is connected to the TCK pin on all devices that share the same data stream.
TMS	1	4	<b>Test Mode Select</b> This is the JTAG mode signal that establishes appropriate TAP state transition for the target devices which share the same data stream
INIT	4	14	<b>Initialize</b> This pin is available for general purpose I/O such as TRST (Test Reset) control or WE (Write-Enable) for FLASH memory.
Vref	7	2	<b>Target Reference Voltage</b> This pin should be connected to a voltage bus on the target system that supplies the JTAG interface.
GND	6	1, 3, 5, 7, 9, 11, 13	<b>Digital Ground</b> All odd-numbered pins on the ribbon cable should be connected to digital ground, reducing crosstalk to a minimum.