

JEM_DIMM/SODIMM™

JTAG External Modules for DIMM/SODIMM Socket Test

InfoSheet FSC

MAIN FEATURES

The StarTest **JEM_DIMM/SODIMM** modules main features are:

- ✓ Performs both Interconnect and Cluster tests for a wide range of DIMM/SODIMM DDR2 and DDR3 memory sockets
- ✓ Supports both external (via header) and in-circuit (via DIMM/SODIMM socket) TAP connection
- ✓ Tests for opens on PWR and GND pins of the DIMM/SODIMM sockets
- ✓ Each I/O pin is independently controlled for sense, drive, bi-directional, and tri-state function
- ✓ Keyed flat connector compatibility
- ✓ Hot Swap: each module may be connected/disconnected between tests without switching power off
- ✓ Equipped with the JTAG/IEEE 1149.1 Test Access Port (TAP)
- ✓ Full software support both for usage and the self-test
- ✓ Full compatibility with the Flynn Systems' **onTAP** Series 4000 
- ✓ Supports the wide range of DIMM, microDIMM, SODIMM, SOCDIMM, and SORDIMM socket formats (consult **StarTest** for additional sockets):

| Module Name | Ordering Part Number | Family Name |
|--------------------------|----------------------|----------------------------|
| ■ 72 pin SODIMM | JEM_SODIMM72 | SODIMM |
| ■ 100 pin SODIMM | JEM_SODIMM100 | SODIMM |
| ■ 144 pin SODIMM | JEM_SODIMM144 | SODIMM |
| ■ 200 pin SODIMM | JEM_SODIMM200 | SODIMM |
| ■ 204 pin SODIMM | JEM_SODIMM204 | SODIMM |
| ■ 200 pin SORDIMM | JEM_SORDIMM200 | SODIMM |
| ■ 200 pin SOCDIMM | JEM_SOCDIMM200 | SODIMM |
| ■ 168 pin DIMM | JEM_DIMM168 | DIMM |
| ■ 184 pin DIMM | JEM_DIMM184 | DIMM |
| ■ 240 pin DIMM | JEM_DIMM240 | DIMM |
| ■ 240 pin UDIMM | JEM_UDIMM240 | DIMM |
| ■ 244 pin miniDIMM | JEM_mDIMM244 | miniDIMM |
| ■ 144 pin microDIMM | JEM_uDIMM144 | microDIMM |
| ■ 172 pin microDIMM | JEM_uDIMM172 | microDIMM |
| ■ 214 pin microDIMM | JEM_uDIMM214 | microDIMM |
| ■ 240 pin VLP RDIMM | JEM_VLP-RDIMM240 | VLP-DIMM |
| ■ 240 pin VLP DIMM | JEM_VLP-DIMM240 | VLP-DIMM |
| ■ 200 pin VLP SORDIMM | JEM_VLP-SORDIMM200 | VLP-SORDIMM |
| ■ 244 pin VLP mini-RDIMM | JEM_VLP-mRDIMM244 | VLP-miniDIMM |
| ■ 244 pin VLP miniDIMM | JEM_VLP-mDIMM244 | VLP-miniDIMM |
| ■ CompactFlash Module | JEM_FlashCard | (form factor- upon demand) |

OVERVIEW

The primary function of the JTAG External Modules (JEM) for the DIMM/SODIMM Socket Cluster Test is to provide test access to off-board signals that otherwise could not be accessed by a JTAG test system and to strengthen the memory-independent JTAG testing for the assembly correctness of the almost all DIMM/SODIMM socket types.

For many designs, JTAG test has adequate access to on-board signals, but signals that go off the board often cannot be tested. By adding JTAG access to memory socket off-board signals, a **JEM_DIMM/SODIMM** module can increase the board's fault coverage, possibly reducing the need for developing alternative tests to reach the required test coverage level. The **JEM_DIMM/SODIMM** module provides a number of JTAG accessible individually controlled test channels that can be used to control and observe signals that go off the board.

It is possible to test the DIMM/SODIMM socket assembly correctness by inserting a DIMM/SODIMM memory module into the corresponding socket and executing a JTAG memory-pattern test. For the usage of this technique the specific memory JTAG test module have to be utilized for write/read memory operations and test results diagnostics. This test offers appropriate results but suffers from the following restrictions:

- ❖ only the socket pins that used for the memory-under-test (MUT) module are tested; another pins (memory depth, configuration control, etc.) may be out of the test;
- ❖ there is no overall power and ground pins testing;

- ❖ the socket pin failure diagnostics depends on the MUT module model and is very limited;
- ❖ the board-under-test DFT failures (memory clocks, etc.) may cause the impossibility to use this technique;
- ❖ it might be time consuming for the big MUT testing.

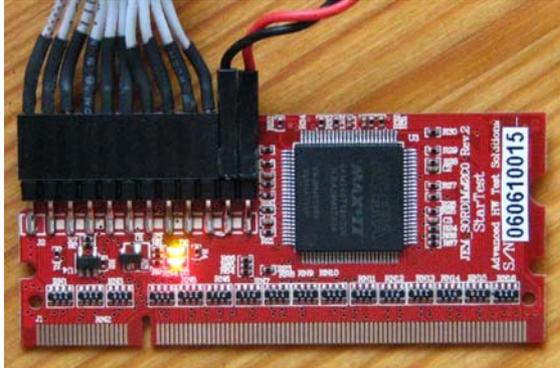


Figure 1. JEM_SORDIMM200 Module

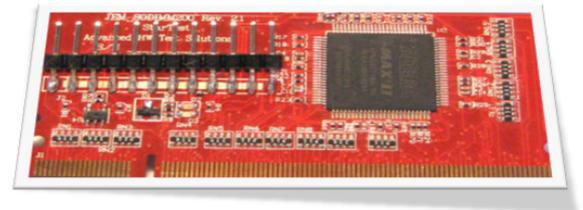


Figure 2. JEM_SODIMM200 Module

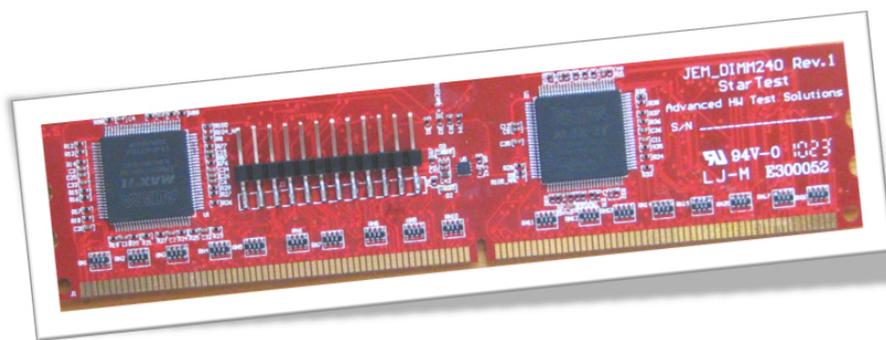


Figure 3. JEM_DIMM240 Module

The usage of the **JEM_DIMM/SODIMM** modules do not know any of the problems mentioned above, and the JTAG test fault coverage level is meaningfully better. These modules provide full bi-directional JTAG controllability and observability for all socket pins. The ATPG tools of any JTAG test platform can generate tests with the advanced diagnostics for the socket pins failure detection, as well as sensing analog voltages on the individual power pins (such as Vdd, Vddq, Vddspd and Vref). The socket test time became neglectable and the test might be the part of the common board Interconnect test. The **JEM_DIMM/SODIMM** module TAP channel can be combined with the board TAP chains or used as a separate TAP.

Two possible DIMM/SODIMM JTAG test setups – external and in-circuit - are shown on Fig. 4 and 5. Each **JEM_DIMM/SODIMM** module is equipped with the external header, so the external test setup, as on Figure 4, is always acceptable. It is obvious, that the usage of the in-circuit test setup, as on Figure 5, requires insertion of the DIMM/SODIMM socket into the in-circuit JTAG chain on early stages of the board-under-test schematics development. The obvious advantages of the in-circuit test setup that might be critical for some test applications are:

- saving one additional TAP channel;
- no use the additional external TAP cable.

In order to get the required pin-out for the in-circuit test set connection for each type of the **JEM_DIMM/SODIMM** modules please consult **StarTest**.

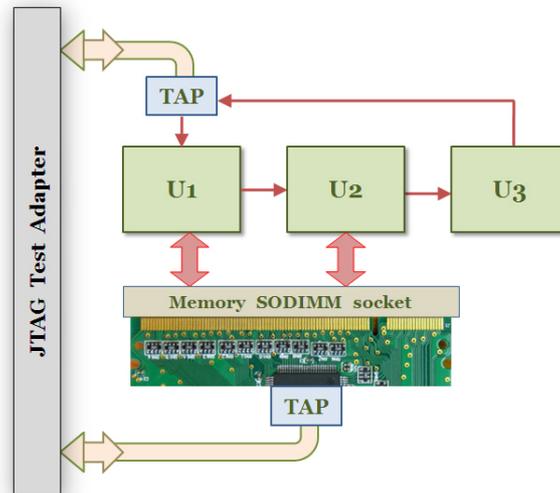


Figure 4. DIMM/SODIMM JTAG test setup with external TAP cable

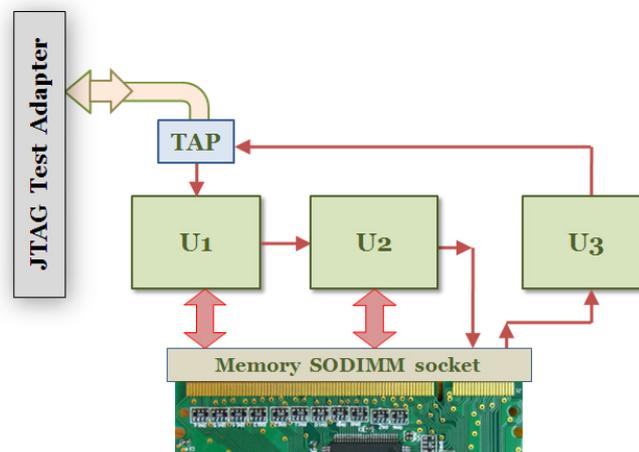


Figure 5. DIMM/SODIMM JTAG completely in-circuit test setup without external TAP cable

One additional important feature of the **JEM_DIMM/SODIMM** modules usage is the opportunity to make an exhaustive structural test of the VTT termination resistors connected to the Address bus and control nets of the DIMM/SODIMM memory card (Figure 6). Particularly, if these resistors are controlled by the IBM microprocessor PPC460EX, all corresponding pins are JTAG-outputs only, and the JTAG test of the VTT termination resistors is impossible without a **JEM_DIMM/SODIMM** usage.

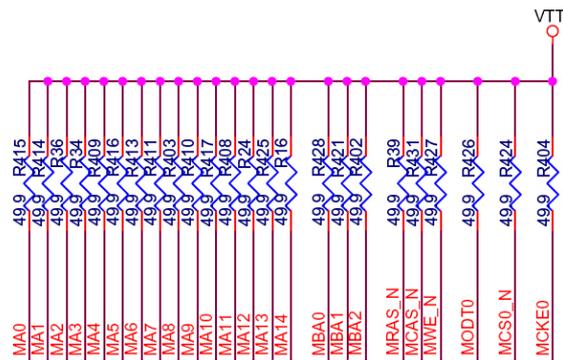


Figure 6. Example of the DIMM/SODIMM VTT termination resistors

JEM_DIMM/SODIMM MODULES INSTALLATION

The **JEM_DIMM/SODIMM** product consists of the following components:

- JEM-DIMM/SODIMM Module with the appropriate module's BSDL file
- JEM Adapter Cable (if required)

Each **JEM_DIMM/SODIMM** module and the JEM Adapter Cable (if required) provide a simple and easy-to-use TAP connection. Such a connection can be used as additional TAP in any multi-TAP JTAG test configuration (at least two TAP configuration, as shown on Figure 4) through any appropriate header, extension cables or flying leads, or in the single-TAP JTAG test configuration without external cabling (in-circuit test setup, see Figure 5, the board-under-test DFT dependable).

In the case of the simultaneous usage of more than one **JEM_DIMM/SODIMM** module in a multi-TAP configuration, each **JEM_DIMM/SODIMM** module should be separately connected to the intended TAP port. Another option is to connect a number of **JEM_DIMM/SODIMM** modules to only one TAP port via the StarTest **JEM_Chain** cable (see Figure 7) that is delivered upon demand.

If the number of separate DIMM/SODIMM sockets to be tested is X, the number the TAP channels of the target board is Y, and X+Y more than the number of accessible TAP ports of your JTAG controller, it is recommended the remake the board-under-test DFT or to use the StarTest's TAP extender module **TAP-Di** that is delivered upon demand.

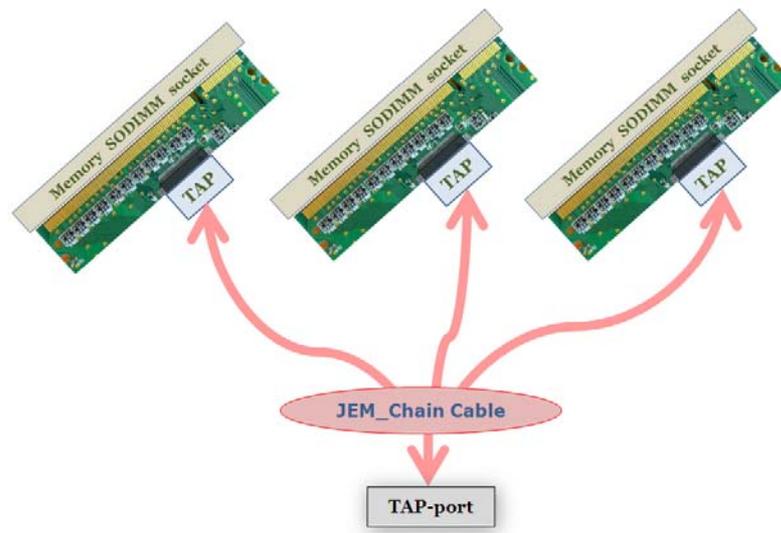


Figure 7. JEM_Chain cable diagram