

Expert JTAG Test Development

Proprietary test development procedures include:

- * Design for Testability (DFT) recommendations during design and for board redesigns
- * Flynn Systems' Interconnect Test
- * Cluster test model development for testing of non-JTAG memory and flash devices
- * Expert evaluation of your board test results and online assistance with debug.
- * BSDL syntax verification to IEEE 1149.1b Boundary Scan Specification

Our test development process takes advantage of your working knowledge of your board designs and our onTAP JTAG test development expertise to produce the highest quality tests, quickly and economically.

When you send us your BSDL and CAD netlist files, plus data sheets for any non-JTAG memory and FLASH devices you want to test, we will work closely with you via e-mail and telephone to develop your onTAP boundary scan tests. When you are ready to apply the tests to the board, we are at your service to assist you as you debug your test, and revise it as necessary to deal with unanticipated board-level and device interactions.

From our experience in developing hundreds of successful boundary scan tests with customers all over the world, we have found this methodology produces the most consistent, successful test results.

Overview of the Test Development Procedure

Step 1. You send us your board netlist, BSDLs, and data sheets for any non-JTAG devices you want to include as a cluster test. Cluster testing non-JTAG devices can boost your overall fault coverage tremendously.

Step 2. We generate the test program and the cluster test device models for devices on your board. This step usually requires some back-and-forth with you to set jumpers and guards to deal with the various interactions between devices on your board.

Step 3. You apply the tests to the board at your facility and let us assist in your test and board debugging. We can show you how to use onTAP's diagnostic tools to get visibility into the state of each boundary cell at each scan vector, and single-step through the test. We can assist you in interpreting the diagnostics and edit/regenerate the tests as required.

Pricing and Lead Time

Pricing for this service is dependent upon the complexity of your board. For a pricing estimate, please send us:

Board netlist

BSDL files for all boundary scan devices on your board.

Data sheets for any non-JTAG devices that you wish to cluster test.

Test development lead time ranges depending upon the complexity of the board and the number of cluster test models required.

Highlights: Licenses

- Cost effective
- Rapid, expert test development with full technical support
- Responsive technical support available for:
 - Design
 - Development
 - Prototyping
 - Manufacturing
- Reliable tests and services for the entire product life cycle.

Expert JTAG Test Development

Proprietary test development procedures include:

- * Design for Testability (DFT) recommendations during design and for board redesigns
- * Flynn Systems' onTAP-Specific Interconnect Test
- * Cluster test model development for testing of non-JTAG memory and flash devices
- * Expert evaluation of your board test results and online assistance with debug.
- * BSDL syntax verification to IEEE 1149.1b Boundary Scan Specification

Our test development process takes advantage of your working knowledge of your board designs and our onTAP JTAG test development expertise to produce the highest quality tests, quickly and economically.

When you send us your BSDL and CAD netlist files, plus datasheets for any non-JTAG memory and FLASH devices you want to test, we will work closely with you via email and telephone to develop your onTAP boundary scan tests. When you are ready to apply the tests to the board, we are at your service to assist you as you debug your test, and revise it as necessary to deal with unanticipated board-level and device interactions.

From our experience in developing hundreds of successful boundary scan tests with customers all over the world, we have found this methodology produces the most consistent, successful test results.

Overview of the Test Development Procedure

Step 1. You send us your board netlist, BSDLs, and datasheets for any non-JTAG devices you want to include as a cluster test. Cluster testing non-JTAG devices can boost your overall fault coverage tremendously.

Step 2. We generate the test program and the cluster test device models for devices on your board. This step usually requires some back-and-forth with you to set jumpers and guards to deal with the various interactions between devices on your board.

Step 3. You apply the tests to the board at your facility and let us assist in your test and board debugging. We can show you how to use onTAP's diagnostic tools to get visibility into the state of each boundary cell at each scan vector, and single-step through the test. We can assist you in interpreting the diagnostics and edit/regenerate the tests as required.

Pricing and Lead Time

Pricing for this service is dependent upon the complexity of your board. For a pricing estimate, please send us:

Board netlist

BSDL files for all boundary scan devices on your board.

Datasheets for any non-JTAG devices that you wish to cluster test.

Test development lead time ranges depending upon the complexity of the board and the number of cluster test models required.

Highlights: Licenses

- Cost effective
- Rapid, expert test development with full technical support
- Responsive technical support available for:
 - Design
 - Development
 - Prototyping
 - Manufacturing
- Reliable tests and services for the entire product life cycle.