

# Technical Support

BOUNDARY SCAN SUPPORT

A better way to test

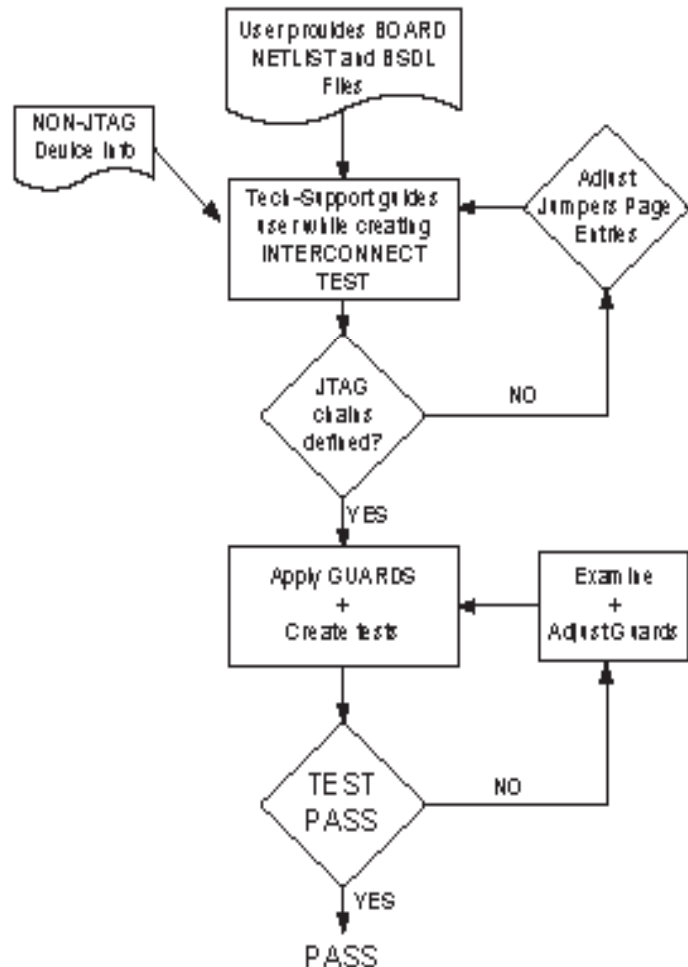
## Features

- Telephone and email support available during business hours.
- Most issues resolved within one business day.
- Telephone and on-line assistance bringing up new applications.
- On-line program updates available for new onTAP builds.
- Assistance with memory/cluster test models.
- Assistance with FLASH programming models.

## Overview

Flynn Systems Technical Support for onTAP can help you get your boundary scan projects up and running quickly! A successful transit through the path in the illustration can be accomplished within a day, often within hours. Given that the source netlist and BSDL files are available and a programming cable is available, the process is straightforward.

Although we encourage onTAP users to bring applications up themselves, our Technical Support can provide detailed interactive assistance during this process so that the time to achieve a 'PASS' is significantly cut.



*Boundary Scan TEST DEVELOPMENT and DEBUG Process. Flynn Systems Tech Support can interactively assist to quickly achieve passing tests.*

## Developing Tests and Bringing Them Online

The development and debug process generally proceeds as discussed in the *Interconnect Test* document, and may include multiple interactive sessions with Tech Support to clarify and assist. After development, if a test fails, onTAP's debug tools may be used to determine the source of the failure. Common reasons for failure include:

- Hookup issues, e.g., power and ground reference lines on the programming cable are not attached.
  - Boundary scan COMPLIANCE pins and TRST pins are not statically held at the correct values.
  - BSDL files don't match logic devices (IDCODE failures)
- Interaction with non-boundary scan logic. Messages within onTAP help to diagnose and correct these problems, of which interaction with non-boundary scan logic is probably the most significant. In this case, onTAP's NetlistBrowser can be used to check the devices that interact with boundary scan pins where failures occur. If a device such as an SRAM is recognized, then steps must be taken to statically guard the output enable pins on the SRAMs so that an SRAM's data bus is not driving while boundary scan pins are also driving on the same nets. Worst case, if

this cannot be done, then some boundary scan test pins must be tri-stated.

Identifying interactive logic, and what steps need to be taken to control it, can usually be accomplished quickly and Flynn Systems Tech Support can assist in this process. Adjusting the guards on the Guards page can usually control the offending circuits. Re-generating and re-running the test should clear up the failures in the problem area.

### Boosting Fault Coverage

Sometimes in the initial pass, fault coverage, as reported by the TestabilitySurvey reports, is not as high as it could be. Measures that can be taken to boost fault coverage include:

- On the Settings page enable the *Self-Capture* option. This allows bidirectional pins, on nets that have only one boundary scan pin, to both drive and capture at the same time. This capability allows such pins and nets to be included in shorts testing and detection.
- On the Settings page, enable *PULLUP and PULLDOWN* resistor tests.
- Use the Jumpers page to make resistors and buffers transparent that lie between boundary scan pins. This allows more boundary scan pins to interact, enhancing coverage.
- Use physical loop backs at connectors to provide more access between boundary scan pins.
- Implement memory and cluster tests to check the connectivity between boundary scan pins and pins on non-boundary scan devices.

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